August 1986 Revised March 2000 DM74LS194A 4-Bit Bidirectional Universal Shift Register

FAIRCHILD

SEMICONDUCTOR

DM74LS194A 4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load

Shift right (in the direction Q_A toward Q_D)

Shift left (in the direction Q_D toward Q_A)

Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is HIGH and S1 is LOW. Serial data for this mode is entered at the shift-right data input. When S0 is LOW and S1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW.

Ordering Code:

Order Number	Package Number	Package Description					
DM74LS194AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow					
DM74LS194AN	DM74LS194AN N16E 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide						
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.							

Features

Parallel inputs and outputs

Synchronous parallel load

Positive edge-triggered clocking

Four operating modes:

Right shift

Do nothing

Direct overriding clear

Left shift

Connection Diagram



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Function Table

Inputs							Outputs						
Clear	Mode		Clock	Serial		Parallel			0.	0	0	0	
	S1	S0	CIOCK	Left	Right	Α	В	С	D	Q _A	QB	Q _C	Q _D
L	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	L	L	L
Н	Х	Х	L	х	Х	Х	Х	Х	Х	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
н	н	н	↑	Х	Х	а	b	с	d	а	b	С	d
н	L	н	Ŷ	х	н	Х	Х	Х	Х	н	Q _{An}	Q _{Bn}	Q _{Cn}
Н	L	н	↑ (х	L	Х	х	Х	Х	L	Q _{An}	Q _{Bn}	Q _{Cn}
Н	н	L	Ŷ	н	Х	х	Х	Х	Х	Q _{Bn}	Q _{Cn}	Q _{Dn}	н
н	н	L	Ŷ	L	Х	Х	Х	Х	Х	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
Н	L	L	Х	х	Х	х	х	Х	Х	Q _{A0}	Q_{B0}	Q_{C0}	Q _{D0}

$$\begin{split} H &= HIGH \, Level \, (steady state) \\ L &= LOW \, Level \, (steady state) \\ X &= Don't Care \, (any input, including transitions) \\ \uparrow &= Transition \, from \, LOW-to-HIGH \, level \\ a, b, c, d &= The \, level \, of \, steady \, state \, input \, at \, input \, A, B, C \, or \, D, \, respectively. \\ Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} &= The \, level \, of \, Q_A, Q_B, Q_C, \, or \, Q_D, \, respectively, \, before the indicated steady state input conditions were established. \\ Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} &= The \, level \, of \, Q_A, Q_B, Q_C, \, respectively, before the most-recent <math display="inline">\uparrow$$
 transition of the clock. \end{split}





PARALLEI. INPUTS

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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Recommended Operating Conditions

Symbol	Parar	neter	Min	Nom	Max	Units	
V _{CC}	Supply Voltage		4.75	5	5.25	V	
V _{IH}	HIGH Level Input Volta	ge	2			V	
V _{IL}	LOW Level Input Volta	ge			0.8	V	
I _{ОН}	HIGH Level Output Cu	rrent			-0.4	mA	
I _{OL}	LOW Level Output Cur	rent			8	mA	
f _{CLK}	Clock Frequency (Note 2)		0		25	MHz	
	Clock Frequency (Note	: 3)	0		20	IVITIZ	
t _W	Pulse Width	Clock	20			ns	
	(Note 4)	Clear	20				
t _{SU}	Setup Time	Mode	30				
	(Note 4)	Data	20			ns	
t _H	Hold Time (Note 4)		0			ns	
t _{REL}	Clear Release Time (N	ote 4)	25			ns	
T _A	Free Air Operating Ten	nperature	0		70	°C	

Note 2: C_L = 15 pF, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 k\Omega, T_A = 25°C and V_{CC} = 5V.

Note 4: $T_A=25^\circ C$ and $V_{CC}=5V.$

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max, V_{IH} = Min$	2.7	3.4		V
V _{OL} LOW Level Output Voltage		$V_{CC} = Min, I_{OL} = Max$ $V_{IL} = Max, V_{IH} = Min$		0.35	0.5	v
		$I_{OL} = 4 \text{ mA}, V_{CC} = Min$			0.4	
1	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			0.1	mA
IH	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ
IL	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
l _{os}	Short Circuit Output Current	V _{CC} = Max (Note 6)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 7)		15	23	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics

Symbol	Parameter	From (Input)	C _L = 50 pF	Units	
		To (Output)	Min	Max	
f _{MAX}	Maximum Clock Frequency		20		MHz
t _{PLH}	Propagation Delay Time	Clock to Any Q		26	
	LOW-to-HIGH Level Output			26	ns
t _{PHL}	Propagation Delay Time	Clock to Any Q		35	
	HIGH-to-LOW Level Output			35	ns
t _{PHL}	Propagation Delay Time	Clear to Any Q		38	
	HIGH-to-LOW Output			38	ns

Note 8: All typicals are at $V_{CC}=5V,\,T_{A}=25^{\circ}C.$

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 10: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Timing Diagram





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0.740 - 0.780

(18.80 - 19.81)

OPTION 01

0.050 ± 0.010

(1.270 ± 0.254) TYP

0.060 (1.524) TYP

0.090

(2.286)

0.250 ± 0.010 (6.350 ± 0.254)

4° TYP

90° ± 4° TYP

0.030 ± 0.015

(0.762 ± 0.381)

0.100 ± 0.010

(2.540±0.254)

TYP

Z

Package Number N16E

OPTIONAL

INDEX AREA

PIN NO. 1

IDENT

16 15 🗌

12

OPTION 02

0.300 - 0.320

(7.620 - 8.128)

95°±5°

0.280 (7.112)

MIN

(0.325^{+0.040} -0.015

(8.255 +1.016

 $\frac{0.065}{(1.651)}$

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0.008 - 0.016 (0.203 - 0.406) TYP

N16E (REV F)

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